CLAIMS

1. A method of operating a cache in a digital computer system, the cache having a plurality of memory locations, the method comprising:

a) obtaining a priority indicator with memory locations in the cache;

b) storing a new item in the cache by:

i) associating a priority with the new item;

ii) selecting a memory location in the cache based in part on the priority indicators of the memory locations in the cache relative to the priority of the new item;

iii) storing the new item in the selected memory location;

c) associating the priority of the new item with the selected memory location in the cache.

2. The method of operating a cache as in claim 1 wherein selecting a memory location in the cache based in part on the priority indicators comprises:

a) when the cache has an empty memory location suitable for storing the new item, storing the new item in an empty memory location;

b) when the cache has no empty memory location suitable for storing the new item, storing the new item in the least frequently used memory location with a priority indicator that is the same or lower than the new item, if one exists, otherwise not storing the new item in the cache and treating the new item as not cacheable.

3. The method of operating a cache as in claim 1 wherein selecting a memory location in the cache based in part on the priority indicators comprises storing the new item in the least frequently used memory location with a priority indicator that is the same or lower than the new item, if one exists.

4. The method of operating a cache as in claim 3 wherein selecting a memory location in the cache based in part on the priority indicators comprises:

a) when the cache has an empty memory location suitable for storing the new item, storing the new item in an empty memory location;

b) when the cache has no empty memory location suitable for storing the new item, storing the new item in the least frequently used memory location with a priority indicator that is lower than the new item.

5. The method of operating a cache as in claim 1 wherein selecting a memory location in cache based in part on the priority indicators comprises:

a) when the cache has an empty memory location suitable for storing the new item, storing the new item in an empty memory location;

b) when the cache has no empty memory location suitable for storing the new item, storing the new item in the least recently used memory location with a priority indicator that is the same or lower than the new item, if one exists, otherwise not storing the new item and treating the new item as not cacheable.

6. The method of operating a cache as in claim 1 wherein selecting a memory location in cache based in part on the priority indicators comprises: storing the new item in the least recently used memory location with a priority indicator that is the same or lower than the new item, if one exists.

7. The method of operating a cache as in claim 6 wherein selecting a memory location in cache based in part on the priority indicators comprises: storing the new item in the least recently used memory location with a priority indicator that is lower than the new item, if one exists.

8. The method of operating a cache as in claim 1 wherein selecting a memory location in cache based in part on the priority indicators comprises: storing the new item in the least recently loaded memory location with a priority indicator that is the same or lower than the new item, if one exists.

9. The method of operating a cache as in claim 8 wherein selecting a memory location in cache based in part on the priority indicators comprises: storing the new item in the least recently loaded memory location with a priority indicator that is lower than the new item, if one exists.

10. The method of operating a cache as in claim 1 wherein selecting a memory location in cache based in part on the priority indicators comprises: storing the new item in a psuedo randomly selected memory location with a priority indicator that is the same or lower than the new item, if one exists.

11. The method of operating a cache as in claim 10 wherein selecting a memory location in cache based in part on the priority indicators comprises: storing the new item in t a psuedo randomly selected memory location with a priority indicator that is lower than the new item, if one exists.

12. The method of operating a cache as in claim 1 wherein the cache contains a data array and a tag array and associating a priority indicator with a memory location comprises storing a value in a field in the tag array.

13. The method of operating a cache as in claim 1 wherein the digital computer system executes a plurality of processes, each process having a priority associated with it and the priority associated with the new item is derived from the priority of the process that generated the new item.

14. The method of operating a cache as in claim 1 additionally comprising:

a) assigning a first priority to a first portion of the plurality of memory locations;

b) assigning a second priority, lower than the first priority, to a second portion of the plurality of memory locations;

c) generating new items to store in the cache with priorities lower than or equal to the second priority; and

d) using the first portion of the plurality of memory locations for non-cache memory operations.

15. The method of operating a cache as in claim 14 wherein the digital computer system comprises a digital signal processor and using the first portion of the plurality of memory locations for non-cache operations comprises using the first plurality of operations for digital signal processing operations.

16. The method of claim 14 wherein assigning a first priority to a first portion of the plurality of memory locations comprises writing to a control register.

17. The method of claim 1 wherein associating a priority with a new item comprises reading a priority from a table associating priorities with memory addresses.

18. The method of claim 1 additionally comprising altering the priority associated with a plurality of memory locations in the cache by writing to a control register.

19. A processor system having a cache, the cache comprising:

a) a data array having a plurality of memory locations for storing items;

b) a tag array having a plurality of memory locations, each location associated with a location in the data array, each location in the tag array having associated therewith:

a first field, indicating a relative priority of the item stored in the associated location in the data array; and

a second field, indicating a portion of an address identifying the item stored in the associated location in the data array.

20. The processor system of claim 19 additionally comprising a memory management unit controlling storage of items in the cache coupled to the tag array whereby locations in the data array are assigned to new items according to a policy in which an empty locations is used, where available, and where no empty location is

available, a location associated with a priority that is the same or less than a priority of the new item.

21. The processor system of claim 20 comprising at least one address bus with a plurality of address bits wherein the cache has an address input with a plurality of address bits coupled to at least a portion of the address bus, and the cache further comprises a plurality of ways, each of the ways having a location in the tag array addressed by a subset of the plurality of address bits, the cache further comprising selection circuitry that, upon application of an address to the address input, couples at least the first fields and second fields associated with the addressed location in each of the tag arrays in each of the ways to the memory management unit.

22. The processor system of claim 19 wherein each location in the tag array additionally l has associated therewith a third field indicating whether a valid item is stored in the associated location in the data array.

23. The processor system of claim 19 additionally comprising a control register having at least one control bit controlling the value stored in the first field of a plurality of memory locations in the tag array.

24. The processor system of claim 19 wherein the cache is implemented in SRAM.

25. The processor system of claim 19 additionally comprising:

a) a memory structure storing priorities associated with addresses; and

b) performance monitoring hardware monitoring a parameter indicative of cache efficiency and dynamically altering priorities stored in the memory structure.

26. A processor system, comprising:

a) a system bus;

b) a semiconductor chip comprising:

i) a processor core;

ii) at least one cache memory coupled to the processor core, the cache comprising a plurality of memory locations for storing items;

iii) a plurality of control bits associated with each memory location in the cache, the plurality of control bits associated with each memory location in the cache, with at least a first control bit for each memory location indicating whether valid information is stored in the memory location and at least a second control bit for each memory location indicating a priority of information stored in the memory location;

iv) a memory management unit coupled to the core, the memory management unit configured to receive as an input at least a first control bit and a second control bit, the memory unit having control outputs connected to the cache, the memory management unit having circuitry implementing a priority based cache replacement policy;

v) an interface to the bus; and

c) semiconductor memory outside the semiconductor chip coupled to the system bus.

27. The processor system of claim 26 wherein the processor core comprises circuitry to execute general purpose microprocessor instructing and digital signal processing functions.

28. The processor system of claim 26 wherein the cache memory is implemented as SRAM and the semiconductor memory is DRAM.

29. The processor system of claim 26 wherein the plurality of control bits additionally comprises a bit for each memory location indicating a replacement policy.

30. The processor system of claim 29 wherein the plurality of control bits additionally comprises a bit for each memory location indicating whether the

information stored in the memory location differs from information stored in a corresponding location in the semiconductor memory.